Electronic Version
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Claims

[c1] 1.An isolation structure of a trench capacitor, the trench capacitor being disposed in a deep trench of a substrate and comprising a conductive layer in the deep trench and a collar oxide layer disposed on a surface of a side-wall of the deep trench, the isolation structure comprising:
a first isolation portion covering the conductive layer and filling a top opening of the deep trench, the first isolation portion having a first thickness; and
a second isolation portion directly contacting the first isolation potion and surrounding the deep trench without overlapping the deep trench, the second isolation portion having a second thickness larger than the first thickness.

[c2] 2.The isolation structure of claim 1, wherein the second isolation portion is disposed by a side of the collar oxide layer, near the conductive layer and the collar oxide layer without being located on the conductive layer and the collar oxide layer.

[c3] 3.The isolation structure of claim 1, wherein a bottom of the second isolation portion is lower than a top of the

collar oxide layer.

[c4] 4.The isolation structure of claim 1 further comprising an isolation liner disposed between the first isolation portion and the conductive layer, the second isolation portion and the conductive layer, and the second isolation portion and the collar oxide layer.

[c5] 5.The isolation structure of claim 4, wherein the isolation liner comprises a nitride liner.

[c6] 6.The isolation structure of claim 4, wherein the isolation liner comprises an oxide liner.

[c7] 7.The isolation structure of claim 1, wherein the first isolation portion and the second isolation portion are oxide layers.

[c8] 8.The isolation structure of claim 1, wherein the first isolation portion and the second isolation portion are oxide layers formed by a high density plasma chemical vapor deposition (HDPCVD) process.

[c9] 9.A method of self-aligned fabricating an isolation structure of a trench capacitor, wherein the trench capacitor is disposed in a deep trench of a substrate having a pad layer thereon, the trench capacitor comprising: a conductive layer filled in the deep trench, wherein a

top surface of the conductive layer and a sidewall of the pad layer define a recess; and

a collar oxide layer disposed on a surface of a sidewall of the deep trench; the method comprising:

forming a mask layer and a dielectric layer in sequence on the substrate and a surface of the recess;

forming a photoresist layer on the dielectric layer, the photoresist layer having an opening that defines a shallow trench;

etching the dielectric layer, the mask layer, and the pad layer through the opening until the substrate is exposed; and

etching the substrate by taking the residual mask layer as a hard mask until a surface of the exposed substrate is lower than a top of the collar oxide layer, wherein the conductive layer and the collar oxide layer remain intact.

[c10] 10.The method of claim 9 further comprising:

removing the photoresist layer, the dielectric layer, and the mask layer so as to form the shallow trench; and

filling the shallow trench with an isolation material.

[c11] 11.The method of claim 10 further comprising performing an oxidation process after forming the shallow trench so as to form a oxide liner on a bottom and a sidewall of the shallow trench.

[c12] 12.The method of claim 11 further comprising forming a nitride liner on the bottom and the sidewall of the shallow trench after forming the oxide liner.

[c13] 13.The method of claim 10, wherein the isolation material comprises silicon oxide.

[c14] 14.The method of claim 13, wherein filling the shallow trench with silicon oxide comprises:
performing a HDPCVD process to deposit a silicon oxide layer on the substrate; and
performing a chemical-mechanical polishing (CMP) process so that a surface of the silicon oxide layer is approximately coplanar with a surface of the pad layer.

[c15] 15.The method of claim 9, wherein the mask layer comprises silicon nitride.

[c16] 16.The method of claim 9, wherein the dielectric layer comprises borosilicate glass (BSG).

[c17] 17.The method of claim 16 further comprising performing a CMP process after depositing the BSG layer.

[c18] 18.The method of claim 9 further comprising depositing an anti-reflection coating (ARC) on the dielectric layer.